G170EG01 V1







Product Specification AU OPTRONICS CORPORATION

Ш	Preliminary Specification
	Final Specification

Module	17.0" SXGA Color TFT-LCD	
Model Name	G170EG01 V1	

Customer	Date
Approved by	
	1.00
Note: This Specification is notice.	subject to change without

Checked & Approved by	Date
Vito Huang	2013/06/24
Prepared by	
Elsie Kuo	2013/06/24
	Business Group / cs corporation





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Record of Revision

Version and Date Page		Old description	New Description		
0.1 2011/01/12	All	First Edition for Customer	All		
0.2 2011/01/14	5	350 (center,Typ)@7.5 mA	350		
	24	Items Required Condition Temperature Humidity Bias (THB) Ta= 50°C., 90%RH, 300hours	Items Required Condition Temperature Humidity Bias (THB) Ta= 50℃, 80%RH, 300hours		
0.3 2011/01/24 1		Hand and the second of the sec	T=40°C,H=95% T=40°C,H=95% T=50°C,H=55% T=70°C		
	26	Thickness= 15.8 mm	Thickness= 18.0 mm		
0.4 2011/04/06 5, 6		Optical ResponseTime= 5 ms	Optical ResponseTime= 30 ms		
	5	This module does not contain an inverter card for backlight.	This module embbededs an LED driver on it.		
	5	Weight: 1800 (g) Typ.	Weight: 1350 (g) Typ.		
	11	4.2 Backlight Unit	4.2 Backlight Unite Rem . Symbol . Min . Max . Unit . Conditions . LED Forward Current . I/ . 120 . (mA) . Note 1,2 .		
	23	No pins drawing of LED driver board	New add pins drawing		
1.0 2011/09/30	6	Without RGB color coordinate	Red xe 0.598 0.648 0.698		
	6	Contrast Ratio	Contrast Ratio		
	24	Without EMI item is RA list	EMI: 30-230 MHz, limit 40 dBu V/m, 230-1000 MHz, limit 47 dBu V/m:		
	25	Outside dimension of carton:434(L)mm*278(W)mm*3 90(H)mm	Outside dimension of carton:426(L)mm*270(W)mm*375(H)m m		
1.1 2012/02/01	5	Operation temperature -30 to +85	Operation temperature -30 to +70		
1.2 2012/05/25	6	No Color Gamut spec	Add Color Gamut 72%		
1.3 2012/07/12		Change View Angle Spec & Delete			





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		View Angle spec(CR=5) View Angle spec(CR=5)		
			Typ. From L85/R85/U80/D80 to L80/R80/U60/D80	
			Min From L70/R70/U70/D70 to L70/R70/U50/D70	
1.4 2013/6/24	2013/6/24 6 Operation temperature -30 to +70 Operation temperature -30 to +85		Operation temperature -30 to +85	
	25	9.2 Carton Package Max capacity: 8 TFT-LCD module per carton Max weight: 14 kg per carton Outside dimension of carton: 426.(L)mm*270 (W)mm*375(H)mm Outside dimension of carton: 426.(L)mm*270 (W)mm*375(H)mm*270 (W)mm*270 (W)mm*	9.2 Carton Package- Max capacity: 8 TFT-LCD module per carton- Max weight: 18 kg per carton- Outside dimension of carton-434(L)mm*278(W)mm*391(H)mm-	
	26	No palletizing info	Add palletizing info	





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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.





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2. General Description

This specification applies to the 17 inch Color TFT-LCD Module G170EG01 V1.

The display supports the SXGA+ $(1280(H) \times 1024(V))$ screen format and 16.7M colors (RGB 6-bits+Hi-FRC data). All input signals are 2 Channel LVDS interface compatible.

This module embbededs an LED driver on it.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 $\ \square$ condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	432 (17.0")
Active Area	[mm]	337.920(H) × 270.336(V)
Pixels H x V		1280 × 3(RGB) × 1024
Pixel Pitch	[mm]	0.264(per one triad) × 0.264
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance	[cd/m ²]	350
Contrast Ratio		800 : 1 (Typ)
Optical ResponseTime	[msec]	30 (Typ)
Nominal Input Voltage VDD	[Volt]	+5.0 (Typ)
Power Consumption (VDD line + LED line)	[Watt]	22 W (Typ.) (with LED driver, all black pattern)
Weight	[Grams]	1350 Typ.
Physical Size (H x V x D)	[mm]	358.5(H) x 296.5(V) Typ. x 18.0(D) Max
Electrical Interface		Dual Channel LVDS
Surface Treatment		Anti-glare type, Hardness 3H
Support Color		16.7M colors (RGB 6-bits +Hi-FRC data)
Temperature Range Operating Storage (Non-Operating)	[°C]	-30 to +85 -30 to +85
RoHS Compliance		RoHS Compliance





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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 $\!\square$ (Room Temperature):

ltem	Unit	Conditions	Min.	Тур.	Max.	Note
Viewing Angle	[degree]	Horizontal (Right) CR = 10 (Left)	70 70	80 80		1
		Vertical (Up) CR = 10 (Down)	50 70	60 80	1-	
Luminance Uniformity	[%]	9 Points	75	80	-	2, 3
		Rising	-	20	25	
Optical Response Time	[msec]	Falling	- <	10	15	4, 6
		Rising + Falling	-	30	40	}
		Red x	0.598	0.648	0.698	
		Red y	0.289	0.339	0.389	
		Green x	0.273	0.323	0.373	
Color / Chromaticity Coordinates		Green y	0.563	0.613	0.663	4
(CIE 1931)		Blue x	0.093	0.143	0.193	_
		Blue y	0.020	0.070	0.120	
		White x	0.263	0.313	0.363	
_		White y	0.279	0.329	0.379	
White Luminance (At LED= 110mA)	[cd/m ²]		280	350	-	4
Contrast Ratio			600	800	-	4
Cross Talk (At 75Hz)	[%]		-	-	1.5	5
Flicker	[dB]		-	-	-20	7
Color Gamut	[%]			72		

Optical Equipment: BM-5A, BM-7, PR880, or equivalent



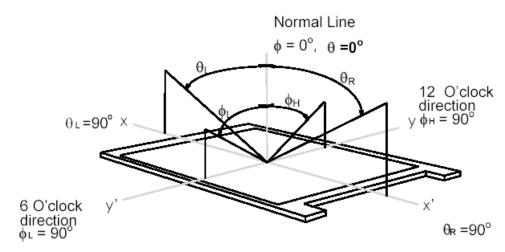


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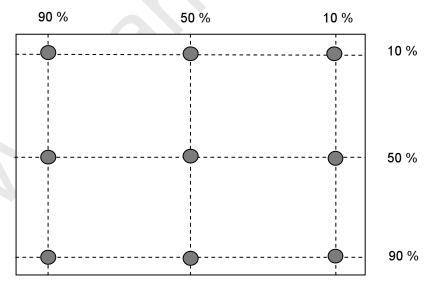
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Note 1: Definition of viewing angle

Viewing angle is the measurement of contrast ratio $\Box 10$, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2: 9 points position



Note 3: The luminance uniformity of 9 points is defined by dividing the maximum luminance values by the minimum test point luminance

δ _{W9} =	Minimum Luminance of 9 points
	Maximum Luminance of 9 points



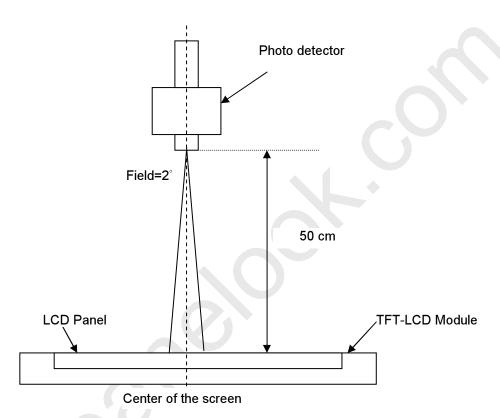


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Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



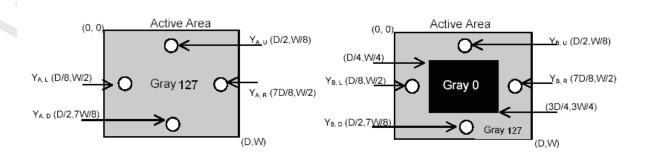
Note 5: Definition of Cross Talk (CT)

 $CT = | YB - YA | / YA \times 100 (\%)$

Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)



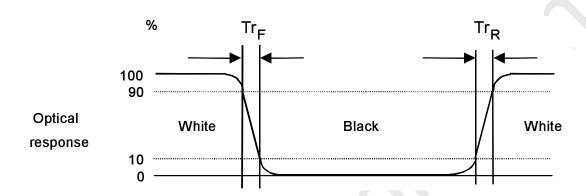




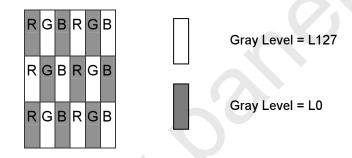
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Note 6: Definition of response time:

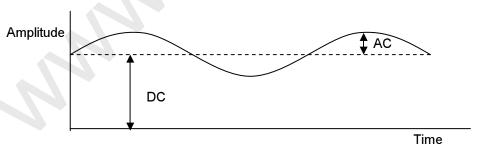
The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time), and from "Full White" to "Full Black" (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 7: Subchecker Pattern



Method: Record dBV & DC value with (WESTAR)TRD-100



Flicker (dB) =
$$20 \log \frac{AC \text{ Level(at 30 Hz)}}{DC \text{ Level}}$$

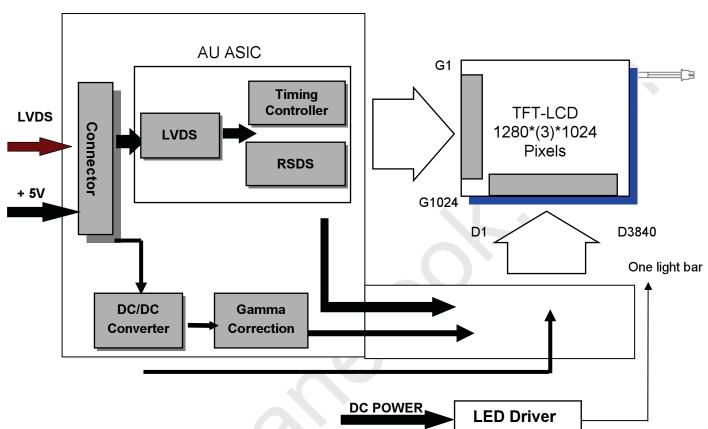




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3. Functional Block Diagram

The following diagram shows the functional block of the 17.0 inches Color TFT-LCD Module:



PCBA Connector:

JAE FI-XB30SSL-HF15 Or Compatible

LED Driver Connector:

3806K-F06Y-03R Or Compatible





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4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 TFT LCD Module

ltem	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VIN	-0.3	6	[Volt]	Note 1,2

4.2 Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
LED Forward Current	I _F	-	120	[mA]	Note 1,2

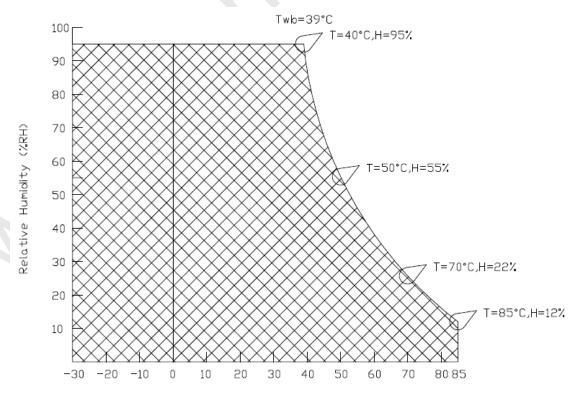
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-30	+85	[°C]	
Operation Humidity	HOP	8	90	[%RH]	Note 2
Storage Temperature	TST	-30	+85	[°C]	Note 3
Storage Humidity	HST	8	90	[%RH]	

Note 1: With in Ta (25 □)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Temperature °C





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5. Electrical characteristics

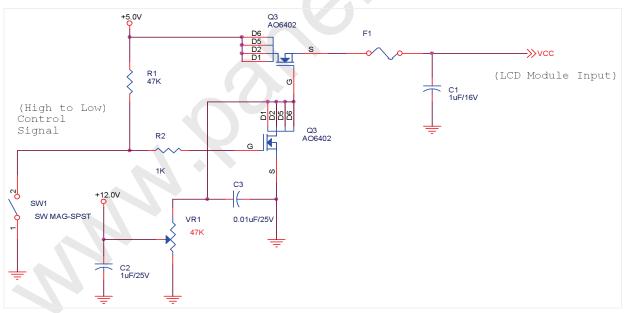
5.1 TFT LCD Module

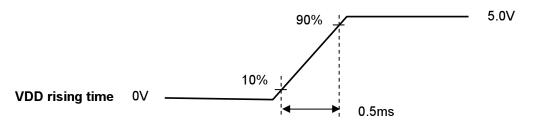
5.1.1 Power Specification

Input power specifications are as follows:

Symble	Parameter	Min.	Тур.	Max.	Unit	Condition
VCC	Logic/LCD Drive Voltage	4.5	5.0	5.5	[Volt]	±10%
ICC	Input Current	-	1.05	1.16	[A]	Vin=5V , All Black Pattern, at 75Hz
IRush	Inrush Current	-	-	3.0	[A]	Note
PCC	VCCPower	-	5.25	5.8	[Watt]	Vin=5V , All Black Pattern, at 75Hz
VCCrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	200	[mV] p-p	With panel loading

Note: Measurement conditions:







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5.1.2 Signal Electrical Characteristics

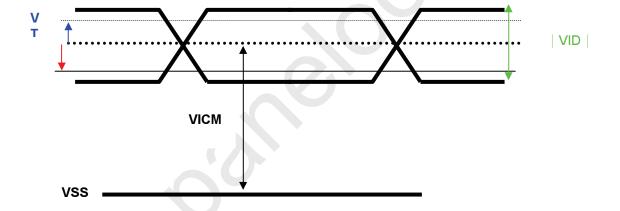
Input signals shall be low or Hi-Z state when Vin is off

It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Each signal characteristics are as follows;

Symbol	Parameter	Min	Тур	Max	Units	Condition
VTH	Differential Input High	_		+100	[m\/]	VICM = 1.2V
VIII	Threshold	-	_	+100	[mV]	Note
\	Differential Input Low	100			[ma] /]	VICM = 1.2V
VTL	Threshold	-100	_	-	[mV]	Note
VID	Input Differential Voltage	100	400	600	[mV]	Note
VICM	Differential Input Common	14.0	14.0	14.5	Γ\ /1	VTH/VTL = ±100MV
VICM	Mode Voltage	+1.0	+1.2	+1.5	[V]	Note

Note: LVDS Signal Waveform







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5.2 Backlight Unit

Parameter guideline LED

Following characteristics are measured under stable condition at 25℃ (Room Temperature)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Remark
V_{LED}	Input Voltage	10.8	12	12.6	Volt	
I _{LED}	Input Current	-	1.18	-	Α	100% Dimming
P _{LED}	Power Consumption	-	14.16	-	Watt	100% Dimming
I _{INRUSH LED}	Inrush Current	-	-	5.1	А	V _{LED} rising time ~ 470us
F _{PWM}	PWM Dimming Frequency	200	-	20K	Hz	
V	Swing Voltage High	4.5	5.0	5.5	Volt	Note 1.2
V _{PWM DIM}	Swing Voltage Low	-	-	0.8	Volt	Note 1,2
D _{PWM}	Dimming Duty Cycle	10	-	100	%	
I _F	LED Forward Current	-	110	-	mA	Ta = 25°℃
V _{LED ON/OFF}	On Control Voltage	3.0	3.3	5.5	Volt	Note 2 4
	Off Control Voltage	-	-	0.8	Volt	Note 3, 4
Operating Life		50000		-	Hrs	Note 5, 6

Note 1: PWM dimming function can be operated by PWM signal. PWM duty cycle can adjust white Luminance.

(PWM High: ON and PWM Low: OFF)

Note 2: PWM signal can not be floating and pull-down to ground when waiting.

Note 3: Enable ($V_{LED\ On/Off}$) must be turned on late than V_{LED} and PWM Signal.

Note 4: Enable ($V_{LED\ On/Off}$) must be turned off early than V_{LED} and PWM Signal.

Note 5: If G170EG01 V1 module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

Note 6: Operating life means brightness goes down to 50% initial brightness. Minimum operating life time is estimated





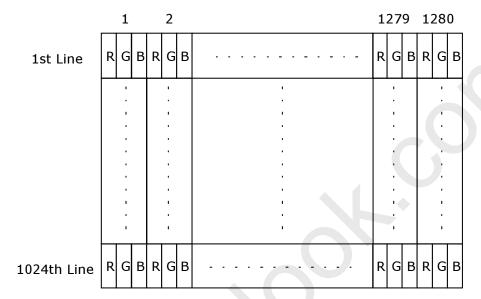
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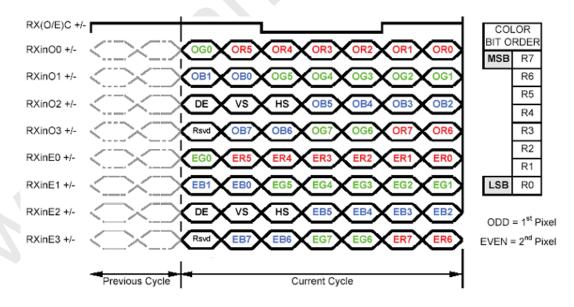
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Note1: Normally, DE, VS, HS on EVEN channel are not used.

Note2: Please follow PSWG.

Note3: 8-bit in





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6.3 Signal Description

The module using a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

PIN# SIGNAL NAME RXO0- Negative LVDS differential data input (Odd data) RXO1- Negative LVDS differential data input (Odd data) RXO2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RXO2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RXOC- Negative LVDS differential clock input (Odd clock) RXOC- Negative LVDS differential clock input (Odd clock) RXO3- Negative LVDS differential clock input (Odd data) RXO3- Negative LVDS differential data input (Odd data) RXO3- Negative LVDS differential data input (Odd data) RXE0- Negative LVDS differential data input (Even data) RXE0- Negative LVDS differential data input (Even data) RXE0+ Positive LVDS differential data input (Even data) RXE1- Negative LVDS differential data input (Even data) RXE1- Negative LVDS differential data input (Even data) RXE1- Negative LVDS differential data input (Even data) RXE2- Negative LVDS differential data input (Even data) RXE2- Negative LVDS differential data input (Even data) RXE2- Negative LVDS differential data input (Even data) RXEC- Negative LVDS differential data input (Even data) RXEC- Negative LVDS differential data input (Even data) RXEC- Negative LVDS differential clock input (Even clock) RXE3- Negative LVDS differential data input (Even data) RXE3+ Positive LVDS differential data input (Even data) RXE3+ Positive LVDS differential data input (Even data) POWER Ground POWER Ground NO Contact			
2 RxO0+ Positive LVDS differential data input (Odd data) 3 RxO1- Negative LVDS differential data input (Odd data) 4 RxO1+ Positive LVDS differential data input (Odd data) 5 RxO2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RxO2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 GND Power Ground 8 RxOC- Negative LVDS differential clock input (Odd clock) 9 RxOC+ Positive LVDS differential clock input (Odd clock) 10 RxO3- Negative LVDS differential data input (Odd data) 11 RxO3+ Positive LVDS differential data input (Odd data) 12 RxE0- Negative LVDS differential data input (Even data) 13 RxE0+ Positive LVDS differential data input (Even data) 14 GND Power Ground 15 RxE1- Negative LVDS differential data input (Even data) 16 RxE1+ Positive LVDS differential data input (Even data) 17 GND Power Ground 18 RxE2- Negative LVDS differential data input (Even data) 19 RxE2+ Positive LVDS differential data input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxE3- Negative LVDS differential clock input (Even clock) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground 26 GND Power Ground	PIN#	SIGNAL NAME	DESCRIPTION
RxO1- Negative LVDS differential data input (Odd data) RxO1+ Positive LVDS differential data input (Odd data) RxO2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RxO2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) RxOC+ Positive LVDS differential clock input (Odd clock) RxOC- Negative LVDS differential clock input (Odd clock) RxO3- Negative LVDS differential data input (Odd data) RxO3- Negative LVDS differential data input (Odd data) RxO3+ Positive LVDS differential data input (Odd data) RxE0- Negative LVDS differential data input (Even data) RxE0+ Positive LVDS differential data input (Even data) RxE1- Negative LVDS differential data input (Even data) RxE1- Negative LVDS differential data input (Even data) RxE1+ Positive LVDS differential data input (Even data) RxE2- Negative LVDS differential data input (Even data) RxE3- Negative LVDS differential clock input (Even clock) RxE3- Negative LVDS differential clock input (Even data) RxE3- Negative LVDS differential data input (Even data) Power Ground Power Ground Power Ground Power Ground (For AUO test Aging+HVS mode)	1		
4 RxO1+ Positive LVDS differential data input (Odd data) 5 RxO2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RxO2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 GND Power Ground 8 RxOC- Negative LVDS differential clock input (Odd clock) 9 RxOC+ Positive LVDS differential clock input (Odd data) 10 RxO3- Negative LVDS differential data input (Odd data) 11 RxO3+ Positive LVDS differential data input (Even data) 12 RxE0- Negative LVDS differential data input (Even data) 13 RxE0+ Positive LVDS differential data input (Even data) 14 GND Power Ground 15 RxE1- Negative LVDS differential data input (Even data) 16 RxE1+ Positive LVDS differential data input (Even data) 17 GND Power Ground 18 RxE2- Negative LVDS differential clock input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential data input (Even data) 22<	2		
5 RxO2- Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 6 RxO2+ Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG) 7 GND Power Ground 8 RxOC- Negative LVDS differential clock input (Odd clock) 9 RxOC+ Positive LVDS differential clock input (Odd data) 10 RxO3- Negative LVDS differential data input (Odd data) 11 RxCO3+ Positive LVDS differential data input (Even data) 12 RxE0- Negative LVDS differential data input (Even data) 13 RxE0+ Positive LVDS differential data input (Even data) 14 GND Power Ground 15 RxE1- Negative LVDS differential data input (Even data) 16 RxE1+ Positive LVDS differential data input (Even data) 17 GND Power Ground 18 RxE2- Negative LVDS differential data input (Even data) 19 RxE2+ Positive LVDS differential clock input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxE3- Negative LVDS differential data input (Even data)	3		
RxO2+ Positive LVDS differential data input (Odd data, H-Sync, V-Sync, DSPTMG) RXOC- Negative LVDS differential clock input (Odd clock) RxOC+ Positive LVDS differential clock input (Odd clock) RxO3- Negative LVDS differential data input (Odd data) RxO3+ Positive LVDS differential data input (Odd data) RxE0- Negative LVDS differential data input (Even data) RxE0+ Positive LVDS differential data input (Even data) RxE1- Negative LVDS differential data input (Even data) RxE1- Negative LVDS differential data input (Even data) RxE1+ Positive LVDS differential data input (Even data) RxE2- Negative LVDS differential data input (Even data) RxE2- Negative LVDS differential data input (Even data) RxE2+ Positive LVDS differential data input (Even data) RxE2+ Positive LVDS differential clock input (Even clock) RxEC- Negative LVDS differential clock input (Even clock) RxE3- Negative LVDS differential clock input (Even data) RxE3- Negative LVDS differential clock input (Even data) RxE3- Negative LVDS differential clock input (Even data) RxE3- Negative LVDS differential data input (Even data) RxE3- Negative LVDS differential data input (Even data) RxE3- Negative LVDS differential data input (Even data) Positive LVDS differential data input (Even data) RxE3- Negative LVDS differential data input (Even data) Positive LVDS differential data input (Even data) Positive LVDS differential data input (Even data)	4	RxO1+	Positive LVDS differential data input (Odd data)
RXOC- Positive LVDS differential clock input (Odd clock) RXOC+ Positive LVDS differential clock input (Odd clock) RXO3- Negative LVDS differential data input (Odd data) RXO3+ Positive LVDS differential data input (Odd data) RXE0- Negative LVDS differential data input (Even data) RXE0- Positive LVDS differential data input (Even data) RXE0+ Positive LVDS differential data input (Even data) RXE1- Negative LVDS differential data input (Even data) RXE1- Negative LVDS differential data input (Even data) RXE1- Positive LVDS differential data input (Even data) RXE1- Positive LVDS differential data input (Even data) RXE2- Negative LVDS differential data input (Even data) RXE2- Negative LVDS differential data input (Even data) RXE2+ Positive LVDS differential clock input (Even clock) RXEC- Negative LVDS differential clock input (Even clock) RXE3- Negative LVDS differential clock input (Even data) RXE3- Negative LVDS differential data input (Even data) Positive LVDS differential data input (Even data) RXE3- Positive LVDS differential data input (Even data) Power Ground GND Power Ground Power Ground Power Ground Power Ground Power Ground (For AUO test Aging+HVS mode)	5	RxO2-	Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
8 RxOC- Negative LVDS differential clock input (Odd clock) 9 RxOC+ Positive LVDS differential clock input (Odd clock) 10 RxO3- Negative LVDS differential data input (Odd data) 11 RxO3+ Positive LVDS differential data input (Even data) 12 RxE0- Negative LVDS differential data input (Even data) 13 RxE0+ Positive LVDS differential data input (Even data) 14 GND Power Ground 15 RxE1- Negative LVDS differential data input (Even data) 16 RxE1+ Positive LVDS differential data input (Even data) 17 GND Power Ground 18 RxE2- Negative LVDS differential data input (Even data) 19 RxE2+ Positive LVDS differential clock input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	6	RxO2+	Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
9 RxOC+ Positive LVDS differential clock input (Odd clock) 10 RxO3- Negative LVDS differential data input (Odd data) 11 RxO3+ Positive LVDS differential data input (Odd data) 12 RxE0- Negative LVDS differential data input (Even data) 13 RxE0+ Positive LVDS differential data input (Even data) 14 GND Power Ground 15 RxE1- Negative LVDS differential data input (Even data) 16 RxE1+ Positive LVDS differential data input (Even data) 17 GND Power Ground 18 RxE2- Negative LVDS differential data input (Even data) 19 RxE2+ Positive LVDS differential data input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential clock input (Even data) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	7	GND	Power Ground
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11 RxO3+ Positive LVDS differential data input (Odd data) 12 RxE0- Negative LVDS differential data input (Even data) 13 RxE0+ Positive LVDS differential data input (Even data) 14 GND Power Ground 15 RxE1- Negative LVDS differential data input (Even data) 16 RxE1+ Positive LVDS differential data input (Even data) 17 GND Power Ground 18 RxE2- Negative LVDS differential data input (Even data) 19 RxE2+ Positive LVDS differential data input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential clock input (Even clock) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	9	RxOC+	Positive LVDS differential clock input (Odd clock)
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RxE0+ Positive LVDS differential data input (Even data) Power Ground RxE1- Negative LVDS differential data input (Even data) RxE1+ Positive LVDS differential data input (Even data) RxE1+ Power Ground RxE2- Negative LVDS differential data input (Even data) RxE2- Negative LVDS differential data input (Even data) RxE2+ Positive LVDS differential data input (Even data) RxEC- Negative LVDS differential clock input (Even clock) RxEC- Positive LVDS differential clock input (Even clock) RxE3- Negative LVDS differential data input (Even data) RxE3+ Positive LVDS differential data input (Even data) RxE3+ Power Ground GND Power Ground Power Ground (For AUO test Aging+HVS mode)	11	RxO3+	Positive LVDS differential data input (Odd data)
14 GND Power Ground 15 RxE1- Negative LVDS differential data input (Even data) 16 RxE1+ Positive LVDS differential data input (Even data) 17 GND Power Ground 18 RxE2- Negative LVDS differential data input (Even data) 19 RxE2+ Positive LVDS differential data input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential clock input (Even clock) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	12	RxE0-	Negative LVDS differential data input (Even data)
15 RxE1- Negative LVDS differential data input (Even data) 16 RxE1+ Positive LVDS differential data input (Even data) 17 GND Power Ground 18 RxE2- Negative LVDS differential data input (Even data) 19 RxE2+ Positive LVDS differential data input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential clock input (Even clock) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	13	RxE0+	Positive LVDS differential data input (Even data)
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18 RxE2- Negative LVDS differential data input (Even data) 19 RxE2+ Positive LVDS differential data input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential clock input (Even clock) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	16	RxE1+	Positive LVDS differential data input (Even data)
19 RxE2+ Positive LVDS differential data input (Even data) 20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential clock input (Even clock) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	17	GND	Power Ground
20 RxEC- Negative LVDS differential clock input (Even clock) 21 RxEC+ Positive LVDS differential clock input (Even clock) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	18	RxE2-	Negative LVDS differential data input (Even data)
21 RxEC+ Positive LVDS differential clock input (Even clock) 22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	19	RxE2+	Positive LVDS differential data input (Even data)
22 RxE3- Negative LVDS differential data input (Even data) 23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	20	RxEC-	Negative LVDS differential clock input (Even clock)
23 RxE3+ Positive LVDS differential data input (Even data) 24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	21	RxEC+	Positive LVDS differential clock input (Even clock)
24 GND Power Ground 25 GND Power Ground (For AUO test Aging+HVS mode)	22	RxE3-	Negative LVDS differential data input (Even data)
25 GND Power Ground (For AUO test Aging+HVS mode)	23	RxE3+	Positive LVDS differential data input (Even data)
	24	GND	Power Ground
26 NC No contact	25	GND	Power Ground (For AUO test Aging+HVS mode)
	26	NC	No contact
27 GND Power Ground		GND	
28 VCC +5.0V Power Supply			
29 VCC +5.0V Power Supply			
30 VCC +5.0V Power Supply		vcc	

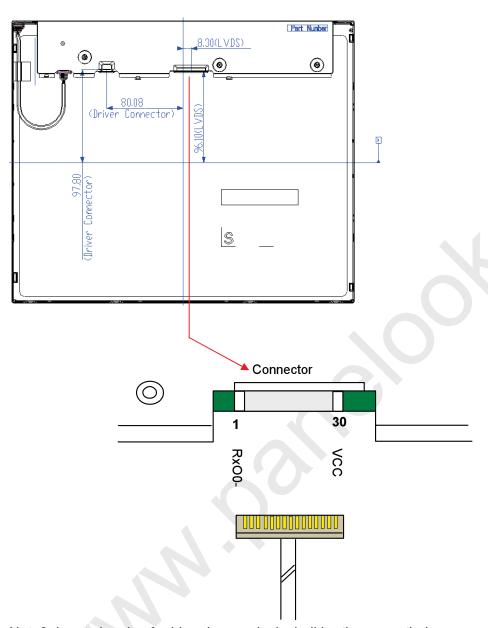




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Note1: Start from left side



Note2: Input signals of odd and even clock shall be the same timing.

Note3: Please follow PSWG.





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6.4 Timing Characteristics

6.4.1 Timing Characteristics

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS82DGG (Texas Instruments) or equivalent.

Signal	ltem	Symbol	Min	Тур	Max	Unit
	Period	Τv	1034	1066	2048	Th
Vertical	Active	Tdisp(v)	1024	1024	1024	Th
Section	Blanking	Tbp(v)+Tfp(v)+PWvs	10	42	1024	Th
	Period	Th	750	844	2048	Tclk
Horizontal	Active	Tdisp(h)	640	640	640	Tclk
Section	Blanking	Tbp(h)+Tfp(h)+PWhs	110	204	1408	Tclk
	Period	Tclk	14.81	18.52	25	ns
Clock	Frequency	Freq	40	54	70	MHz
Frame rate	Frame rate	F	49	60	76	Hz

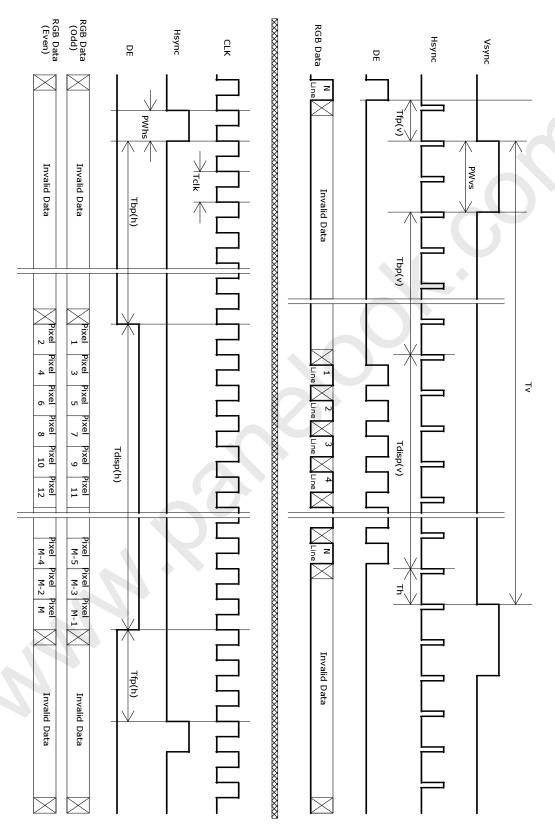
Note : DE mode only





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6.4.2 Timing Diagram







Global LCD Panel Exchange Center

Product Specification

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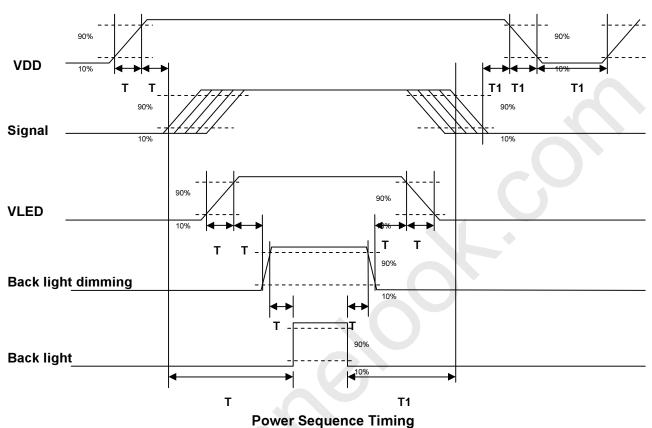
[ms]

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6.5 Power ON/OFF Sequence

T13

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Value Parameter Unit Min. Max. Тур. 0.5 10 T1 [ms] T2 30 40 50 [ms] T3 200 [ms] T4 0.5 10 [ms] T5 10 [ms] T6 10 [ms] **T7** 0 [ms] T8 10 [ms] T9 10 [ms] T10 110 [ms] T11 0 16 50 [ms] T12 10 [ms]

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7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

7.1.1 Connector

Connector Name / Designation	Interface Connector
Manufacturer	JAE or Compatible
Type Part Number	FI-XB30SSL-HF15 or Compatible
Mating Housing Part Number	JAE FI-X30HL or Compatible

7.1.2 Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	RxOIN0-	2	RxOIN0+
3	RxOIN1-	4	RxOIN1+
5	RxOIN2-	6	RxOIN2+
7	GND	8	RxOCLKIN-
9	RxOCLKIN+	10	RxOIN3-
11	RxOIN3+	12	RxEIN0-
13	RxEIN0+	14	GND
15	RxEIN1-	16	RxEIN1+
17	GND	18	RxEIN2-
19	RxEIN2+	20	RxECLKIN-
21	RxECLKIN+	22	RxEIN3-
23	RxEIN3+	24	GND
25	GND (AGMODE+HVS)	26	NC
27	GND	28	VCC
29	VCC	30	VCC





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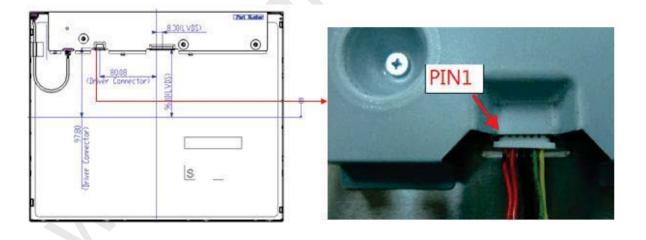
7.2 Backlight Unit

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	Lamp Connector
Manufacturer	E&T or compatible
Connector Model Number	3806K-F06Y-03R or compatible
Mating Connector Model Number	H208K-P06N-02B or compatible

7.2.1 Signal for LED driver connector

Pin#	Symbol	Signal Name
1	VCC	12V
2	VCC	12V
3	GND	GND
4	GND	GND
5	Display on	5V-On / 0V-Off
6	Dimming	PWM Dimming







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Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50□, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 85□, 300hours	
Low Temperature Operation (LTO)	Ta= -30□, 300hours	
High Temperature Storage (HTS)	Ta= 85□, 300hours	
Low Temperature Storage (LTS)	Ta= -30□, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20□/30min, 60□/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD	Contact Discharge: \pm 8KV, 150pF(330 Ω) 1sec, 8 points, 25 times/ point.	4
ESD	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	ı
ЕМІ	30-230 MHz, limit 40 dBu V/m, 230-1000 MHz, limit 47 dBu V/m	
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

Note1: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost Self-recoverable. No hardware failures.

Note2:

- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.
- No function failure occurs.





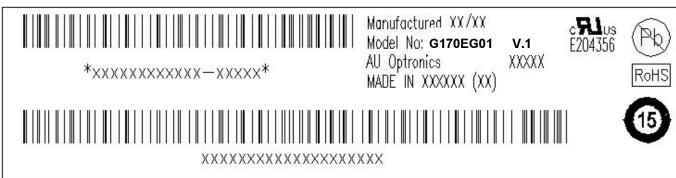
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9. Label and Packaging

9.1 Shipping Label (on the rear side of TFT-LCD display)

The shipping label format is shown as below.

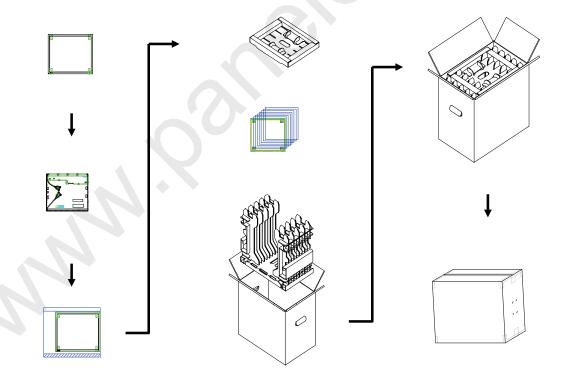


9.2 Carton Package

Max capacity: 8 TFT-LCD module per carton

Max weight: 18 kg per carton

Outside dimension of carton: 434(L)mm*278(W)mm*391(H)mm



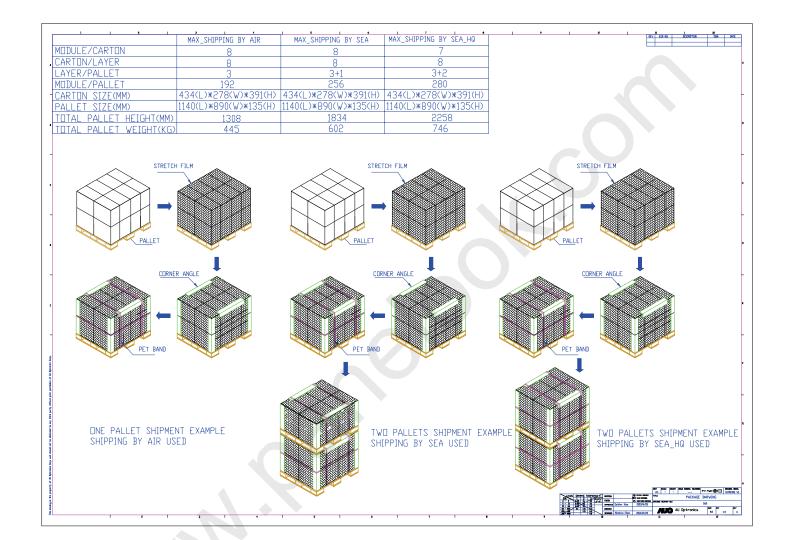




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9.3 Palletizing







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10. Mechanical Characteristics

